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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,506	10/20/2003	Huajie Chen	FIS920030241US1	4303

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,506	CHEN ET AL	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-9* is/are allowed.

6)☒ Claim(s) *1-6,10-18 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's remarks filed December 11, 2006. Applicant's arguments have been fully considered and are persuasive. The final rejection has been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1,10, 12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Hachimine et al. (U.S. 7,105,394).

4. Hachimine (e.g. Fig. 3, 37) discloses:

(cl. 1, 10, 12) a method of manufacturing a semiconductor structure, comprising the steps of forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate; etching regions of the pFET structure and the nFET structure (e.g. forming gate etc.); forming a pFET stack in the pFET channel and an nFET stack in the nFET channel (Fig. 6); providing a first layer (e.g. 24b; Fig. 37) of material at substrate in the regions of the pFET structure / and source/drain regions (12) associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state

(Abstract) within the pFET channel; and providing a second layer of material (24a) at the substrate in the regions of the nFET structure and source/drain regions (12) associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state(Abstract) at the nFET channel;

(cl. 15) where the first and second material are raised above a surface of the substrate (e.g. Fig. 37).

5. Claims 10, 12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffman et al. (U.S. 2004/0253776).

6. Hoffman (Fig. 2) discloses:

(cl. 10, 12) a method of manufacturing a semiconductor structure, comprising the steps of: forming a p-type field-effect-transistor (pFET) channel (132) and a n-type field-effect-transistor (nFET) channel (130) in a substrate; forming a pFET structure and an nFET structure on the substrate associated with the pFET channel and the nFET channel, respectively; etching regions of the pFET structure and the nFET structure; after the pFET stack is formed, forming a first material (214) with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress (Par. 0026) in the pFET channel; after the nFET stack is formed, forming a second material (213) with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress

(Par. 0026) in the nFET channel; and doping source and drain regions (203; Par. 0023) of the nFET and pFET structures;

(cl. 15) where the first and second material are raised above a surface of the substrate (Fig. 5).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. (U.S. 2004/0253776).

9. Hoffman discloses the elements stated in paragraph 6 of this office action, but fails to disclose the thickness of the first and second layer being 10 to 100nm.

10. However, applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, the selected dimension would have been obvious to one of ordinary skill in the art, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir.

1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

11. Claims 10-12, 17 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. (U.S. 2004/0253776) in combination with Yeo et al. (U.S. 6,923,913).

12. Hoffman discloses the elements stated in paragraph 6 of this office action, but does not explicitly disclose the material used for its stress layer or that its layer is SiGe and Si:C.

13. Yeo teaches use of SiGe and Si:C to produce tensile and compressive stress.

14. It would have been obvious to one of ordinary skill in the art to form the first and second layers of Hoffman as SiGe and/ or Si:C in order to provide stress layers as required by Hoffman ("suitable material"; Par. 0021).

15. Furthermore with respect the material being relaxed or the selection of either SiGe or Si:C, the selected claimed material would have been obvious to one of ordinary skill in the art, since the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See M.P.E.P 2144.07.

16. Claims 1-5, 11-12, 14-18 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. (U.S. 6,923,913).

17. Yeo (e.g. Fig. 6A-8D) discloses:

(cl. 1, 10, 22) a method of manufacturing a semiconductor structure, comprising the steps of forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate (e.g. invention forming gate etc for cmos; Col. 1, Lines 25-27 & 54-55); etching regions/ channel of the pFET structure and the nFET structure (e.g. 8B) forming a pFET stack in the pFET channel and an nFET stack in the nFET channel (e.g. Fig. 6A-C); providing a first layer (e.g. 505) of material at substrate in the regions of the pFET structure / and source/drain regions (504) associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state (CLAIM 12 of Yeo) within the pFET channel; and providing a second layer of material[1] at the substrate in the regions of the nFET structure and source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state (CLAIM 10 of Yeo) at the nFET channel;

(cl. 2) the first layer of material is SiGe (Col. 7, Lines 45-48);

(cl. 3) the second layer of material is Si:C. (Col. 7, Lines 45-48);

(cl. 14, 15) where the first and second material are embedded in the substrate and raised above the substrate (e.g. 8C);

(cl. 18) in situ doping of the first and second material (Col. 9, Lines 34-36);

(cont. cl. 22) growing layer in the channel (Fig. 5);

[1] Similar process applied for transistors in CMOS

(cl. 23) before growing material in channels it has a lattice constant different than a base lattice (e.g. SiGe/ Si:C[2]) constant of the substrate;

(cl. 24) the channels about the pFET stack and the channels about nFET stack are formed by etching (Col. 9, Lines 1-2);

(cl. 25) wherein the channels about the pFET stack and the channels about the nFET comprise source/drain regions (Fig. 8B-C).

18. With respect to the contents and selection of material of claims 2, 4, 5 and 17 that its Ge is approximately greater than 0% in ratio to Si or wherein its Si:C has a content of C of about 4% or less.

19. Furthermore with respect the material being relaxed or the selection of % selection of either Si or C, the selected claimed material would have been obvious to one of ordinary skill in the art, since the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See M.P.E.P 2144.07.

20. With respect to the thickness in claims 5, 10 and 16 that the first and second layers of material is formed at a thickness of between about 10 to 100 nm. See paragraph 10 of this office action.

21. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. (U.S. 6,923,913) in combination with Parks (U.S.

[2] Same material as claimed

22. Yeo discloses the elements stated in paragraph 17 of this office action, but fails to explicitly disclose use of a mask over channel region, etching of its substrate and the growing of its strain layers within the regions.

23. Parks utilizes a mask (208) for etching ("t"; Fig. 5C) and Langdo (Fig. 5) utilizes mask (36) for growing a material (100)[3].

24. It would have been obvious to one of ordinary skill in the art to incorporate the use of a mask with the process of Yeo in order to etch and grow material at selected regions as taught by Parks (e.g. etched according to pattern) and Langdo (e.g. material grown in exposed window).

Allowable Subject Matter

25. Claims 7-9 are allowed.

Response to Arguments

26. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone

[3] Likewise, Parks shows forming material at selected region due ot mask (Fig. 5A-B).

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D.
January 7, 2007

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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